REMARKS

Claims 1 through 15 are currently pending in the application.

This amendment is in response to the Office Action of June 20, 2002.

Claims 1 through 9 and 11 through 15 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kinoshita (JP 58-90728).

Claims 8 and 10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Deguchi (JP 62-18714).

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 1 through 9 and 11 through 15 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kinoshita (JP 58-90728).

Kinoshita discloses a positioning mark on a semiconductor wafer characterized by at least two regions where a plurality of fine indentations having *an arc-shaped cross-sectional form* are arranged in specified positions on the main face of a semiconductor wafer. A third region, which is flat, extends between the two regions. (Kinoshita, claim 1)

Presently amended independent claim 1 recites an overlay target with "at least one trench having a bottom surface, said one trench including a series of *substantially vertically extending raised lines originating at said bottom surface of said trench.*"

Presently amended independent claim 5 recites an overlay target with "at least one pad area having a bottom surface, said one pad area including a series of *substantially vertically extending raised lines originating at said bottom surface of said pad area.*"

Presently amended independent claim 8 recites an overlay target "having a bottom surface comprising at least one series of substantially vertically extending raised lines *originating at said bottom surface of said overlay target.*"

Applicants respectfully submit that Kinoshita does not anticipate the instant invention recited in presently amended independent claims 1, 5 and 8 under 35 U.S.C. § 102 because each and every element as set forth therein is not found, either expressly or inherently described in Kinoshita. In particular, Kinoshita does not disclose, teach or suggest a trench, a pad area or an overlay target which includes at least a series of *substantially vertically extending raised lines originating at the bottom surface of* a trench, a pad area or an overlay target. Rather, Kinoshita discloses regions having plurality of fine indentations having an arc-shaped cross-sectional form. Clearly, the minute cavities disclosed in Kinoshita do not include *substantially vertically extending raised lines* as specifically claimed in the present invention.

Therefore, Kinoshita does not disclose each and every element of independent claims 1, 5 and 8 as proposed to be amended herein. Accordingly, it is respectfully submitted that independent claims 1, 5 and 8, as proposed to be amended, are not anticipated by Kinoshita.

Further, claims 2 through 4, 6, 7, and 9 through 15 are each allowable, among other reasons, as depending either directly or indirectly from presently amended independent claims 1, 5, and 8, which should be allowed.

Presently amended claims 3, 6, 7, and 9 through 15 are further allowable since Kinoshita does not disclose a series of *substantially vertically extending* raised lines as specifically described and claimed in the present invention.

Claims 8 and 10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Deguchi (JP 62-18714).

Deguchi discloses a method for forming alignment marks comprising a part having high light reflectance and a part having low light reflectance. Etching is performed by means of dry etching to form a finely roughened area on the part of the alignment marks having low

reflectance. More specifically, fine rod-shaped crystals protrusions are formed by dry etching on the portions of a Mo film formed on the substrate of a wafer as shown in Fig. 2.

Presently amended independent claim 8 recites an overlay target "having a bottom surface comprising at least one series of substantially vertically extending raised lines *originating at said bottom surface of said overlay target.*"

Applicants respectfully submit that Deguchi does not anticipate the instant invention recited in presently amended independent claim 8 under 35 U.S.C. § 102 because each and every element as set forth therein is not found, either expressly or inherently described in Deguchi. In particular, Deguchi does not disclose, teach or suggest an overlay target which includes at least one series of substantially vertically extending raised lines *originating at the bottom surface of an overlay target.* Rather, Deguchi discloses forming rod like projections by etching through the entire depth of the Mo film formed on the substrate. Clearly, Deguchi discloses rod like projections that *originate at the top surface of the semiconductor substrate.*

Therefore, Deguchi does not disclose each and every element of independent claim 8 as proposed to be amended herein. Accordingly, it is respectfully submitted that independent claim 8, as proposed to be amended, is not anticipated by Deguchi.

Further, claim 10 is allowable, among other reasons, as depending either directly or indirectly from presently amended independent claim 8, which should be allowed.

Claim 10 is further allowable since Diguchi does not disclose a series of raised lines as specifically described and claimed in the present invention.

For the reasons set forth herein, Applicants submit that claims 1 through 15 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 1 through 15 and the case passed for issue.

Respectfully submitted,

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JRD/sls:djp

Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Amended) An overlay target comprising:

at least one trench having a bottom surface, said one trench including a series of substantially vertically extending raised lines originating at said bottom surface of said trench.

3. (Amended) The overlay target of claim 1, wherein said at least one trench comprises a plurality of trenches defining said overlay target, each of said plurality of trenches includes [a] said series of substantially vertically extending raised lines originating at said bottom surface of said trench.

5. (Amended) An overlay target comprising:

at least one pad area having a bottom surface, said one pad area including a series of substantially vertically extending raised lines originating at said bottom surface of said pad area.

6. (Amended) The overlay target of claim 5, wherein said at least one pad area includes a plurality of pad areas defining said overlay target, each of said plurality of pad areas includes [a] said series of substantially vertically extending raised lines originating at said bottom surface of said pad area.

7. (Amended) The overlay target of claim 6, further comprising at least one trench including [a] said series of substantially vertically extending raised lines originating at said bottom surface of said overlay target.

8. (Amended) A semiconductor wafer comprising:
a semiconductor substrate; and
an overlay target having a bottom surface comprising at least one series of substantially vertically extending raised lines originating at said bottom surface of said overlay target.

9. (Amended) The semiconductor wafer of claim 8, wherein said at least one series of substantially vertically extending raised lines is etched into said semiconductor substrate.

10. (Amended) The semiconductor wafer of claim 8, wherein said at least one series of substantially vertically extending raised lines is etched into a material layer overlying said semiconductor substrate.

11. (Amended) The semiconductor wafer of claim 8, wherein said at least one series of substantially vertically extending raised lines is disposed in at least one trench.

12. (Amended) The semiconductor wafer of claim 11, wherein a plurality of trenches and a corresponding plurality of series of substantially vertically extending raised lines define said overlay target, each of said plurality of trenches includes one of said plurality of series of substantially vertically extending raised lines.

13. (Amended) The semiconductor wafer of claim 8, wherein said at least one series of substantially vertically extending raised lines is disposed in at least one pad area.

14. (Amended) The semiconductor wafer of claim 13, wherein a plurality of pad areas and a corresponding plurality of series of substantially vertically extending raised lines define said overlay target, each of said plurality of pad areas includes one of said plurality of series of substantially vertically extending raised lines.

15. (Amended) The semiconductor wafer of claim 8, wherein said at least one series of substantially vertically extending raised lines comprises a first series of raised lines disposed in a pad area and a second series of raised lines disposed in a trench.